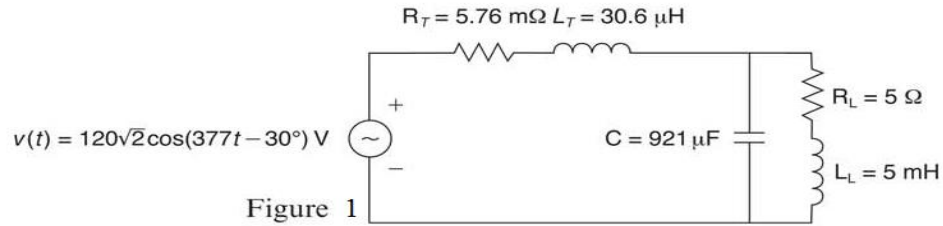
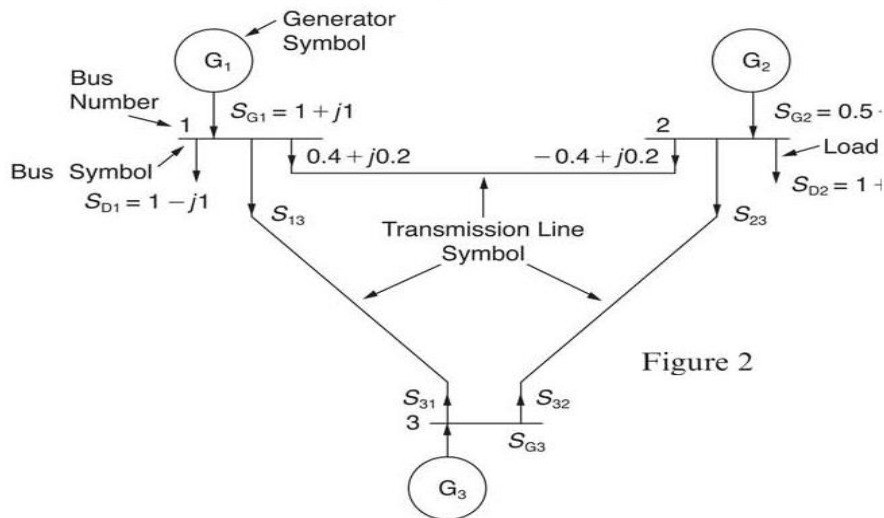


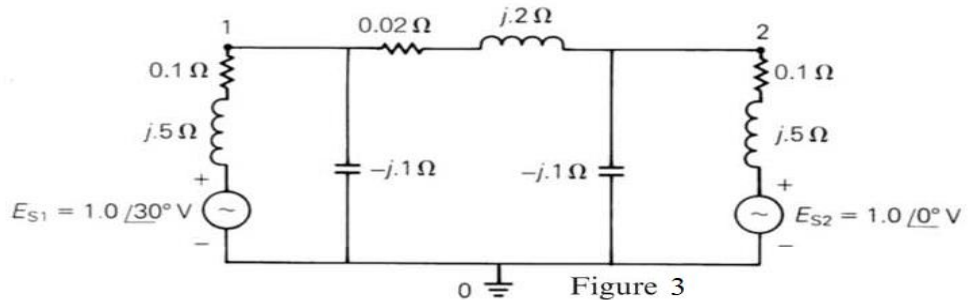
- 1- Consider the circuit shown in Figure 1 in time domain. Convert the entire circuit into phasor domain.



- 2- Modeling the transmission lines as inductors, with  $S_{ij} = S_{ji}^*$ . Compute  $S_{13}$ ,  $S_{31}$ ,  $S_{23}$ ,  $S_{32}$ , and  $S_{G3}$  in Figure 2 (Hint: complex power balance holds good at each bus, satisfying KCL.)



- 3- For the circuit shown in Figure 3, convert the voltage sources to equivalent current sources and write nodal equations in matrix format using bus 0 as the reference bus. Do not solve the equations.



- 4- Determine the  $4 \times 4$  bus admittance matrix  $Y_{bus}$  and write nodal equations in matrix format for the circuit shown in Figure 3. Do not solve

